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Novel Design Approach of 64-bit Full Adder with Sky130 PDK using Open-Source VLSI Tools

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Abstract*— This paper presents the design and implementation of a 64-bit full adder using the SkyWater 130nm Process Design Kit (PDK) and open-source electronic design automation (EDA) tools. The purpose of this research is to develop a highly efficient arithmetic unit suitable for integration in modern digital systems. Utilizing the open-source tools such as Magic-VLSI for layout design, Xscheme and NETGEN for schematic, this paper demonstrates a streamlined design process that underscores the potential of open-source EDA solutions. The designed 64-bit full adder was rigorously tested, and performance metrics were evaluated. The final implementation demonstrated a significant improvement in power efficiency and speed compared to existing designs, with a power consumption of 1.66 uW and a propagation delay of 2.54ns. These results validate the effectiveness of using open-source tools in advanced digital circuit design and highlight the viability of the SkyWater 130nm PDK for high-performance applications.

***Index Terms*— Arithmetic circuit, Open-Source Tools, Sky130 PDK, Xscheme**

I. INTRODUCTION

The increasing demand for high-performance computing has driven the need for efficient arithmetic units, with the 64-bit full adder being a critical component. Traditional CMOS design techniques, while effective, often encounter challenges related to scaling, power efficiency, and design complexity. The SKY 130nm PDK along with other open-source tools offers a novel approach by modularizing the design process, enabling more manageable and optimized implementations.

When it comes to digital circuit design, creating effective arithmetic circuits is essential for a number of applications, including digital communication systems, signal processing units, and microprocessors. With the use of these circuits, one may perform arithmetic operations on binary numbers, including division, multiplication, and addition. Such a circuit is the adder. An adder is a digital logic that performs addition of numbers and gives output in the form of sum and carry in a binary system. The purpose of this research is Two-fold: Firstly, to explore the capabilities of open-source VLSI tools in designing digital arithmetic circuits, and secondly, to provide a comprehensive guide for designing, simulating and implementing such circuits using these tools. Through practical experimentation this research aims to empower individuals interested in digital design to gain hands-on experience with VLSI tools and deepen their understanding of digital arithmetic circuits.

In this research a bottom-to-top approach is adopted to design a 64-bit adder circuit. Beginning at the transistor level there is a meticulous construction of the fundamental logic gates required for addition operations, such as NAND gates, OR gates using SKY130 PDK technology. These gates are then systematically interconnected and organized into functional units, following established design methodologies and principles. As ascending through, these units are designed into larger components, culminating in the creation of the complete 64-bit adder circuit. This bottom-to-top approach ensures a systematic and structured development process, allowing for efficient debugging, optimization and scalability while maintaining a clear understanding of the circuit's underlying architecture. By adhering to this method, the author aims to achieve a robust and reliable 64-bit adder design that meets the research's objectives and performance requirements.

This study explores the development and application of digital arithmetic circuits that make use of open-source VLSI technology. The objective of using these tools is to comprehensively evaluate the entire design flow, including verifying the layout versus the schematic. The paper not only focuses on the theoretical aspects but also on practical considerations such as performance metrics, area efficiency, and power consumption. Utilizing Magic VLSI for layout design and XSchem for schematic capture, fundamental digital logic gates and arithmetic components like half adder, full adder, 8-bit adder and 64-bit adder are designed.

II. LITERARY SURVEY

Over the years, a number of 64-bit complete adders have been created, including the ripple carry adder, carry

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lookahead adder, and carry choose adder. Each adder has their own limitations and strengths. For example, Ripple carry adder requires less area for assembling as compared to other adder circuits. On the contrary it shows signified propagation delay making it less suitable for high-speed or large bit-width applications. On the other hand, 64-bit full adder is more compatible and efficient in comparison to other adders as propagation delay is little reduced. 64-bit full adder at 45nm has very low delay as compared to 90nm and 180nm.

The author aims to achieve a more compact area i.e, area efficiency, low propagation delay and power consumption. Most papers in literature aim to achieve development in 8-bit, 16-bit, 32-bit, 64-bit at different nanometers. The main objective is to design a 64-bit full adder with Sky 130nm PDK using open-source tools. The paper is divided into five sections. Section 3 displays schematic design along with layout designs, section 4 shows the result of the project and section 5 has a conclusion. The following section displays the various open-source tools used in designing of adder, designing rule checking (DRC) along with layout versus schematic LVS) checking methods.

A. Xschem:

XSchem is an effective open-source tool for designing complex digital circuits like a 64-bit full adder due to its robust features, hierarchical design support, and seamless integration with simulation tools. By leveraging these capabilities, designers can efficiently manage and verify large-scale digital designs, ensuring accuracy and performance. The development of a 64-bit full adder in XSchem not only demonstrates the tool's capabilities but also

Provides a solid foundation for further digital design projects.

B. Magic VLSI:

MAGIC VLSI provides a modular framework that simplifies the design of complex VLSI circuits. This section elaborates on the design process of the 64-bit full adder, detailing the key components and their integration. Magic-VLSI is an open-source layout tool used for designing integrated circuits (ICs). It provides a versatile environment for creating physical layouts of digital, analog, and mixed-signal circuits. Magic VLSI offers advanced features for editing, viewing and verifying layouts including support for complex geometries, DRC (Design Rule Checking) and LVS (Layout vs. Schematic) checks. It supports various input and output formats, facilitating interoperability with other EDA tools. Magic VLSI is widely utilized by IC designers, researchers and students for its robust functionality and accessibility.

C. Netgen:

Netgen is an open-source tool used for digital net-list comparisons, verification, and conversion. It accepts various net-list formats and provides functionalities like net-list comparison, equivalence checking and net-list conversion between different formats. VHDL or Verilog are examples of hardware description languages (HDL) that are used to define 64-bit complete adders. The HDL code is synthesized to generate a netlist. It is used to compare the synthesized netlist against the expected logical structure to ensure that the synthesis process has not introduced errors. It can also translate the netlist into different formats required for various simulation and verification tools. Net-gen is commonly used in both analog as well as digital design flows for verifying the correctness of synthesized net-lists.

D. SKY-130 PDK:

The SKY130 Process Design Kit (PDK) is an essential resource for designing integrated circuits (ICs) using the SkyWater Technology Foundry's 130-nanometer (nm) CMOS process. This PDK is comprehensive, offering a wide range of tools and data necessary for the design, simulation, and fabrication of silicon chips. It supports a variety of applications, including mixed-signal, RF, and analog designs, alongside digital logic. Key features of the SKY130 PDK include Design Rule Check (DRC) to ensure adherence to manufacturing constraints, Layout Versus Schematic (LVS) verification for matching physical layouts to schematic designs, and Parasitic Extraction (PEX) for accurate post-layout simulation and performance prediction. Additionally, the PDK provides standard cell libraries, analog and mixed-signal components, process design rules, and detailed simulation models, ensuring robust and efficient design processes.

Design Rule Checking (DRC):

Design Rule Check (DRC) is a critical process in the field of electronic design automation (EDA) that ensures the manufacturability and functionality of semiconductor devices and printed circuit boards (PCBs). DRC is important because it may identify problems with designs early on, which lowers the possibility of expensive mistakes occurring during manufacture. Typically DRC defines rules based on manufacturing capabilities & limitations. The EDA tools applies these rules to the design layout. Further the violation is detected and reporting is done along with their precise location and nature. In continuation violations are reviewed and corrected. Similarly the SKY130 PDK includes rule decks compatible with industry-standard DRC tools, enabling designers to perform comprehensive design rule checks and ensure compliance with Sky-Water's manufacturing requirements.

Layout Versus Schematic (LVS) Checking:

The interplay between schematic and layout design is critical. The layout must accurately reflect the schematic to ensure the fabricated circuit performs as intended. Discrepancies between the schematic and layout can lead to

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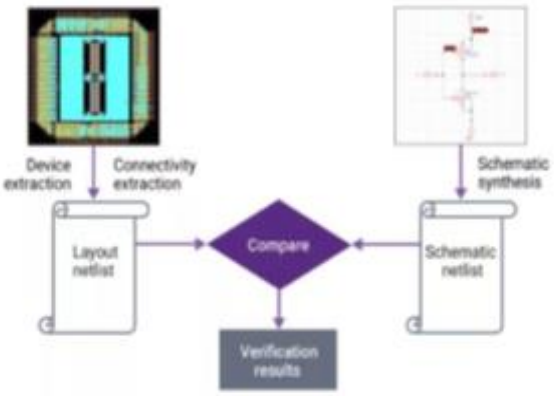
functional failures or suboptimal performance. Layout Versus Schematic (LVS) checks are performed to ensure the layout matches the might require revisiting the schematic to account for parasitic effects and other physical considerations.



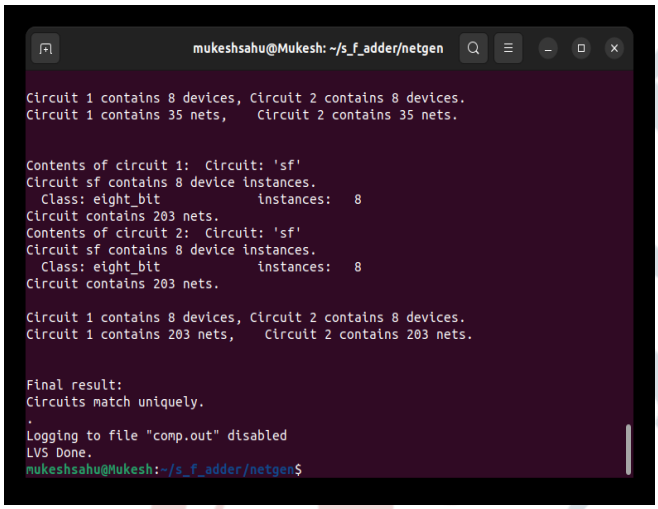


Fig.1.1 LVS for 64-bit adder

III. SCHEMATIC DESIGN FLOW FOR 64-BIT ADDER ALONG WITH LAYOUT DESIGNS

The following is the general workflow for layout design:

- Using the eight-bit adder components in Magic VLSI, design an architecture for a sixty-four bit adder. Arrange the Eight Bit Adder in the active region in accordance with the Sixty Four Bit Adder scheme.
- Ensure that the transistors are positioned correctly and have adequate space between them to prevent interference and ensure proper performance. Utilize metal layers to establish connections between the Eight Bit Adder layout's component parts. To link the transistors' gate, source, and drain terminals, route metal traces in accordance with the schematic design.
- Use Layout vs. Schematic (LVS) and Design Rule Checking (DRC) checks to ensure functional correctness and adherence to design requirements.

Basic Design of Logic GATE:

Logic gates are the building blocks of digital circuitry. Every logic gate performs a basic logical function based on Boolean algebra by operating on one or more binary inputs to produce a single binary output. NAND and OR gates are employed in this situation. A NAND only generates a high output when any gate's input terminal is low. Figure From x to y, which follows, illustrates the schematic, symbol, and arrangement of the NAND gate.

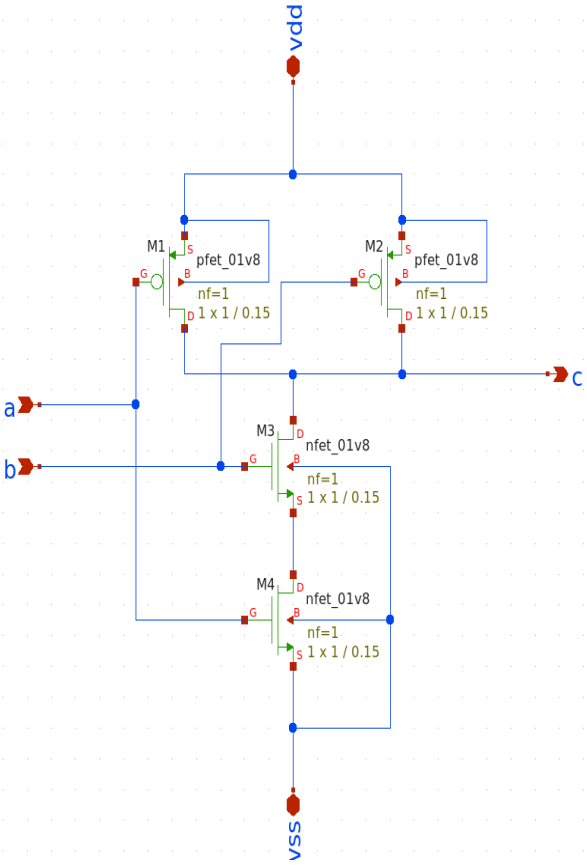


Fig. 1.2 NAND Gate Schematic

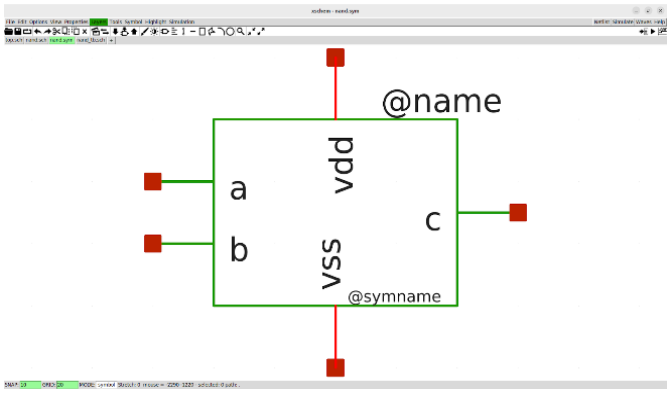


Fig. 1.3 NAND Gate Symbol

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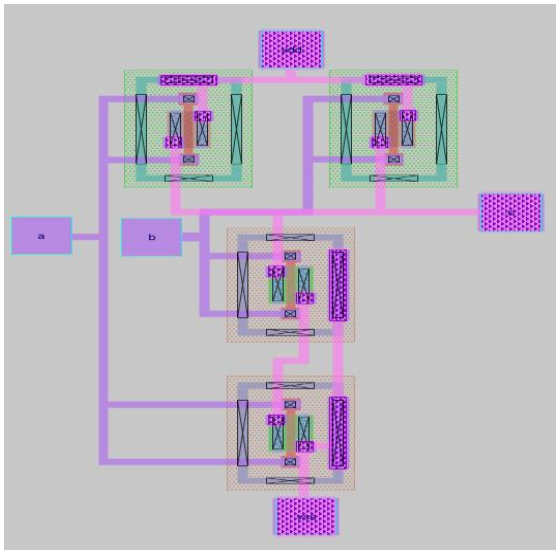

Fig. 1.4 NAND Gate Layout

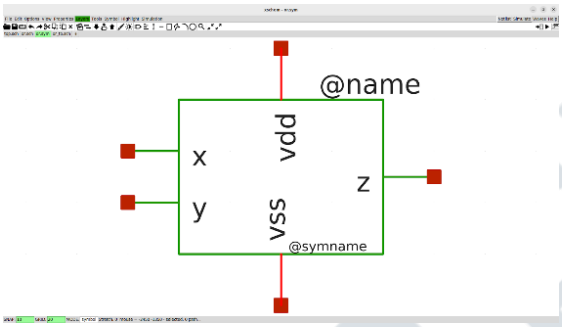

Fig. 1.5 OR gate Symbol

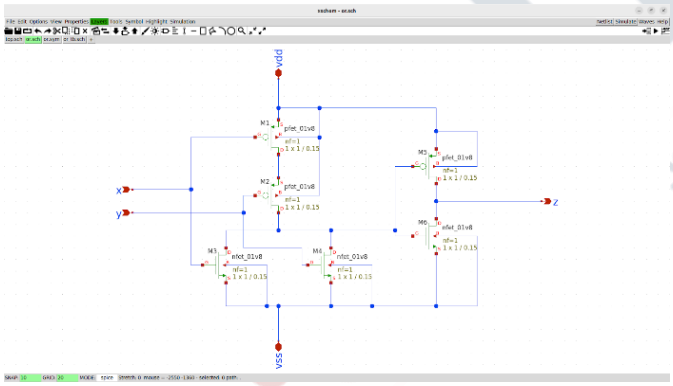

Fig. 1.6 OR gate Schematic

8-bit Adder from Full Adders:

In an 8-bit adder, the addition of two 8-bit binary numbers is carried out using a series of full adders. Each bit addition is handled by an individual full adder, with the least significant bit (LSB) to the most significant bit (MSB) being connected to the corresponding inputs of these adders. Each full adder's carry output is fed into the carry input of the next higher bit full adder. The sum output from each full adder represents the respective bit of the final sum. The total carry-out for the entire 8-bit addition is indicated by the carry output of the last complete adder. Thus, the 8-bit adder is structured with 8 full adders arranged in a cascade, where the inputs are tied to the specific bits of the numbers being added, and the outputs generate the 8-bit result.

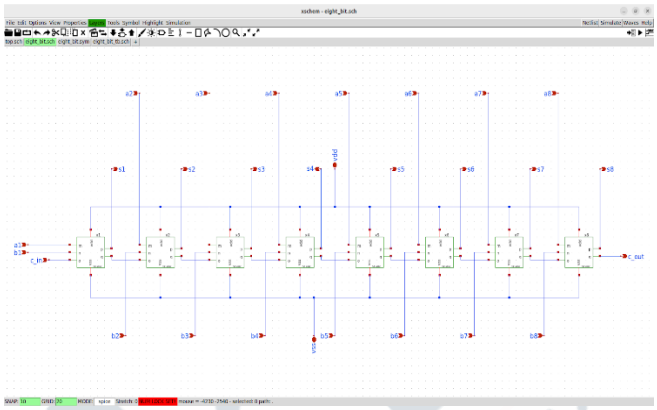

Fig: 1.7 8-bit adder schematic

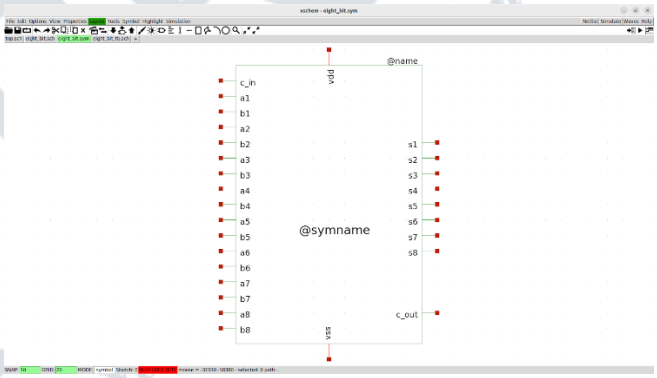

Fig. 1.8: 8-bit symbol

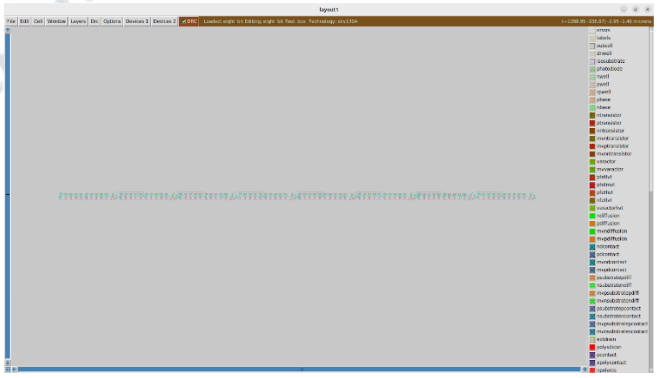

Fig. 1.9: 8-Bit layout

64-bit adder:

A 64-bit adder adds two 64-bit binary numbers together. Implement each segment of the 64-bit addition using an 8-bit full adder. Segment the 64-bit numbers into 8-bit chunks.

Connect corresponding bits (from least significant bit to most significant bit) of both numbers to the inputs of the respective 8-bit full adders. Propagate the carry output (c_out) of each 8-bit full adder to the carry input (c_in) of the

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next higher significant bit's 8-bit full adder. Take the sum output from each 8-bit full adder as the corresponding bits of the output sum. The carry output (C_OUT) of the last 8-bit full adder represents the carry-out for the entire 64-bit addition. The 64-bit adder consists of 8 8-bit full adders connected in a cascade fashion with inputs connected to the respective bits of the input numbers and outputs forming the 64-bit sum.

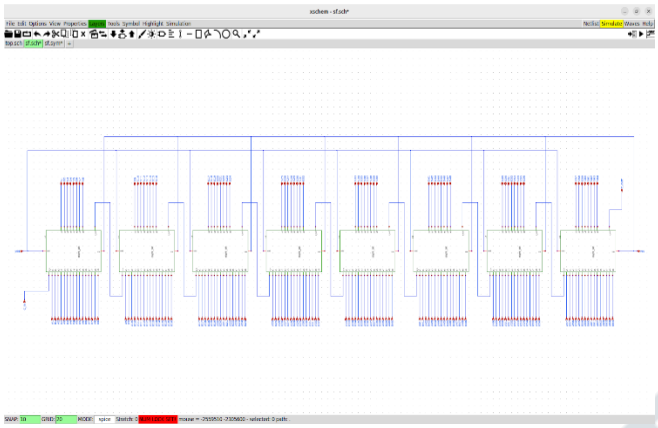

Fig.2.0: 64-bit adder schematic

Fig.2.1: 64-bit adder symbol

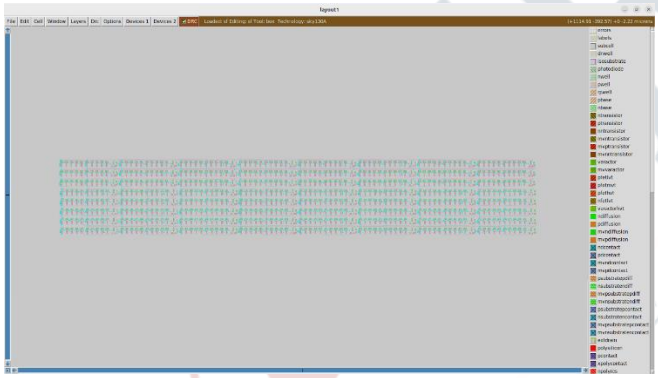

Fig.2.2: 64-bit adder layout

IV. RESULT ANALYSIS

Power analysis, simulation analysis, delay time analysis & area analysis are the major parameters to be focused in this section. The power analysis and delay time analysis were performed using the open-source tool NGSpice. The hierarchical design, netlist generation and schematic was designed using Xschem. To test further area analysis, SKY130 PDK was used. The detailed analytical procedure is as follows.

POWER ANALYSIS:

Power is being analyzed in netgen. Power is crucial to understand design's energy consumption. It is obtained by the formula:

Iavg*Vdd

ie. product of average current flowing from the Vdd branch and the supply voltage (1.8v) over one period of time. In result negative sign shows the absorption of power 1.66µw. Figure shows the output of netgen.

P = Iavg*Vdd
= -1.66µW

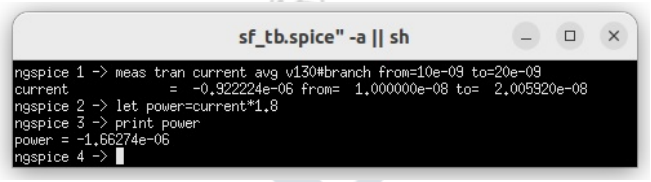

Fig.2.3 Power calculation

SIMULATION ANALYSIS:

To verify the functionality of these circuits, a test bench is generated for a half adder and full adder in Xschem by creating a simulation environment. This will help in validating their operation under the defined input conditions. The pictorial representation of simulation analysis is shown in Fig.2.4 and Fig.2.5.

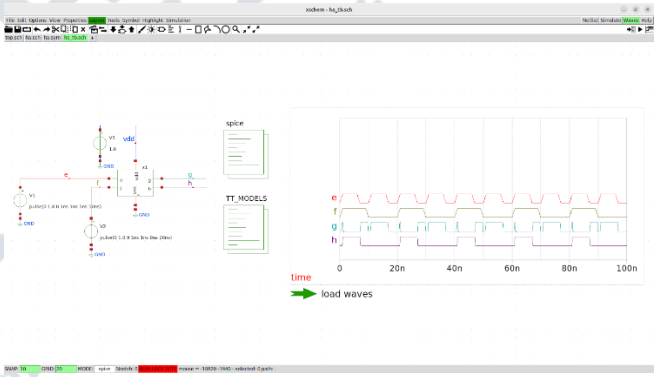

Fig.2.4 Half adder test bench

Fig.2.5 Full Adder Test Bench

III. DELAY TIME ANALYSIS:

Delay time analysis also known as propagation delay refers to evaluating the time taken for the adder to produce the correct output after

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receiving the input signals. It is obtained by taking the average of time taken by signal to travel high to low Tphl and time taken by signal to travel low to high level Tplh. It is obtained by the formula:

Tp = (Tphl+Tplh)/2.

The pictorial representation of delay time analysis is shown in the Fig. Secondly Fig. shows the calculation of delay time analysis of 2.545ns.

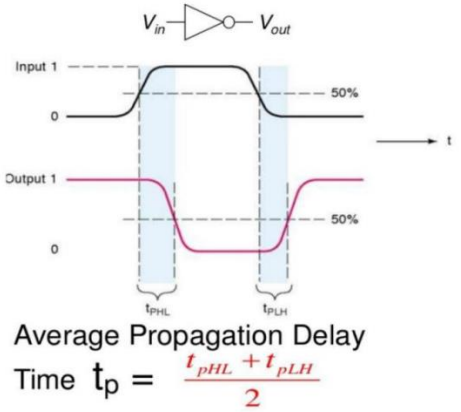

Fig.2.6 Delay time Analysis

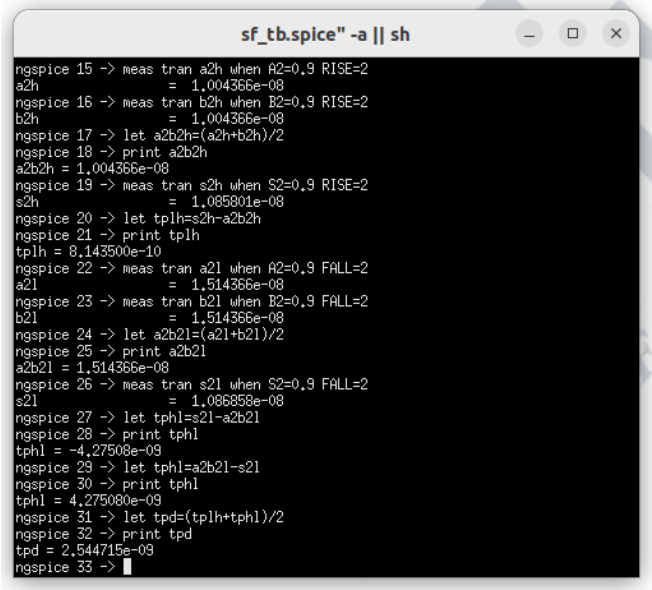

Fig.2.7 Delay calculation of 64-bit full adder

IV. AREA ANALYSIS:

Area analysis of a layout refers to evaluating the physical size or footprint occupied by the circuit design on the semiconductor chip. For a 64-bit adder layout, area analysis provides insights into the layout's size, which is a critical factor influencing chip area utilization, manufacturing cost and overall integration density. Area analysis is being performed by integrating open-source tools Magic VLSI and SKY 130 PDK. At last after verification and design rule check (DRC), area analysis is obtained to be 168170.859 sq nm. The following fig displays the area analysis.

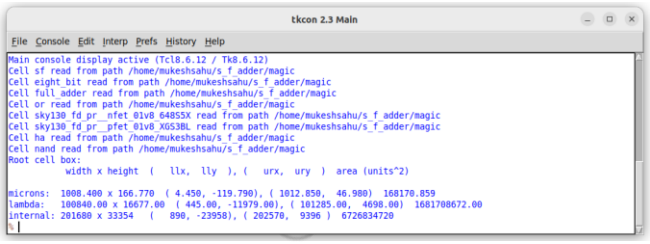

Fig.2.8 Area Calculation of 64-bit Full Adder

Table I. Performance analysis at different technologies of 64-bit Full Adder

Technology(nm)	Power consumption(µw)	Time delay(ns)
180-nm	4.15	0.22
130-nm (Proposed design)	1.66	2.54

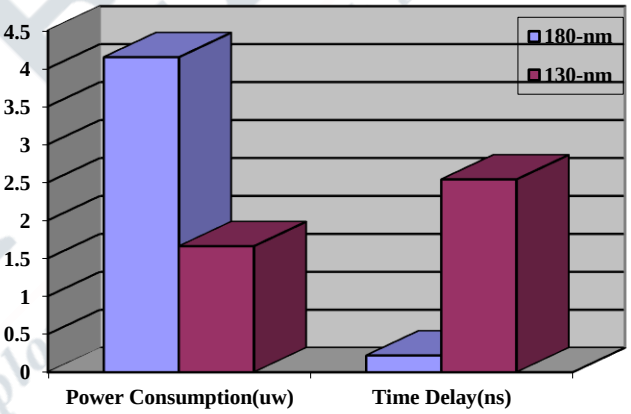

Fig.2.9 Power and delay comparison

V. CONCLUSION

A comprehensive design and execution of 64-bit full adder is tested and proposed in this paper. This research successfully demonstrates the design and implementation of a 64-bit full adder using the Sky130 process technology, leveraging the open-source tools Magic VLSI and Netgen. This research underscored the importance of meticulous design, verification processes like Design Rule Checking (DRC) and Layout vs. Schematic (LVS), and simulation to ensure circuit functionality and compliance with design rules. By minimizing the most of logical components of the design structure, it will be helpful to decrease area and power consumption.

The author claims that the proposed 64-bit full adder at 130nm technology has a power consumption of 1.66µW

along with propagation delay of 2.54ns at area efficiency of 168170.859 sq nm.

This work not only underscores the viability of the SkyWater 130 nm technology for advanced digital circuits but also paves the way for future innovations in the domain of low-power, high-speed arithmetic units. On the basis of this foundation, future studies can investigate additional improvements and applications in more intricate computational systems. From the given proposed design of 64bit full adder, in future 128bit full adder can also be design.

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